Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. – 5. (canceled)

6. (currently amended) A data path circuit in a digital processing device, wherein the data path circuit is coupled to a memory bus for obtaining values from a memory, the data path circuit comprising

a plurality of groups of data lines;

a plurality of data address generators for coupling the plurality of groups of data lines to the memory bus so that a value from the memory transferred by the memory bus can be placed onto a group of data lines;

one or more functional units for performing a digital operation coupled to the plurality of groups of data lines; and

a plurality of ~~registers~~register files, wherein each register file in the plurality of registers is coupled to ~~each~~ a group of data lines in the plurality of data lines ~~on~~ in a one-to-one correspondence, wherein each of the plurality of ~~registers~~ register files ~~selectively~~ store values from the group of data lines in which each of the plurality of register files is coupled~~plurality of groups of data lines so that the values are selectively available on the plurality of groups of data lines~~.

7. (currently amended) The data path circuit of claim 6, wherein 8 groups of 16 data lines are used, wherein each group of data lines is coupled to a register file in the plurality of register files capable of storing 8 16-bit words, wherein each of the data address generators can selectively provide a value on a first group of data lines to a second group of data lines.

8. (currently amended) The data path circuit of claim 1, wherein the functional units include a multiplier and accumulator, the data path circuit further comprising

a coupling of the multiplier to the plurality of data ~~path~~ lines;

a coupling of the accumulator to the plurality of data ~~path~~ lines; and

Amendments to the Claims:

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1. – 5. (canceled)

6. (currently amended) A data path circuit in a digital processing device, wherein the data path circuit is coupled to a memory bus for obtaining values from a memory, the data path circuit comprising

a plurality of groups of data lines;

a plurality of data address generators for coupling the plurality of groups of data lines to the memory bus so that a value from the memory transferred by the memory bus can be placed onto a group of data lines;

one or more functional units for performing a digital operation coupled to the plurality of groups of data lines; and

a plurality of ~~registers~~ register files, wherein each register file in the plurality of registers is coupled to ~~each~~ a group of data lines in the plurality of data lines ~~on~~ in a one-to-one correspondence, wherein each of the plurality of ~~registers~~ register files ~~selectively~~ store values from the group of data lines in which each of the plurality of register files is coupled. ~~plurality of groups of data lines so that the values are selectively available on the plurality of groups of data lines.~~

7. (currently amended) The data path circuit of claim 6, wherein 8 groups of 16 data lines are used, wherein each group of data lines is coupled to a register file in the plurality of register files capable of storing 8 16-bit words, wherein each of the data address generators can selectively provide a value on a first group of data lines to a second group of data lines.

8. (currently amended) The data path circuit of claim 1, wherein the functional units include a multiplier and accumulator, the data path circuit further comprising

a coupling of the multiplier to the plurality of data ~~path~~ lines;

a coupling of the accumulator to the plurality of data ~~path~~ lines; and

direct data lines coupled between the multiplier and the accumulator.

9. (previously presented) The data path circuit of claim 8, wherein the direct data lines are uni-directional for transferring data from the multiplier to the accumulator.

10. (currently amended) A digital processing system comprising

a multiplier;

an accumulator;

a configurable data path coupled to both the multiplier and the accumulator in parallel; and

a direct data path coupled between the multiplier and the accumulator.

11. (new) A data path circuit in a digital processing device, wherein the data path circuit is coupled to a memory bus for obtaining values from a memory, the data path circuit comprising

a plurality of groups of data lines;

a plurality of data address generators for coupling the plurality of groups of data lines to the memory bus so that a value from the memory transferred by the memory bus can be placed onto a group of data lines;

one or more functional units for performing a digital operation coupled to the plurality of groups of data lines; and

a plurality of register files, wherein each register file in the plurality of registers is coupled to a single group of data lines in the plurality of data lines, wherein each of the plurality of register files store values from the group of data lines in which each of the plurality of register files is coupled.

12. (new) The data path circuit of claim 11, wherein 8 groups of 16 data lines are used, wherein each group of data lines is coupled to a register file in the plurality of register files capable of storing 8 16-bit words, wherein each of the data address generators can selectively provide a value on a first group of data lines to a second group of data lines.

13. (new) The data path circuit of claim 11, wherein the functional units include a multiplier and accumulator, the data path circuit further comprising

a coupling of the multiplier to the plurality of data lines;
a coupling of the accumulator to the plurality of data lines; and
direct data lines coupled between the multiplier and the accumulator.

14. (new) The data path circuit of claim 13, wherein the direct data lines are uni-directional for transferring data from the multiplier to the accumulator.

15. (new) The data path circuit of claim 11, further comprising a plurality of registers coupled to the plurality of data path lines, the plurality of registers configured to store values from the plurality of data path lines so that the values are selectively available on the plurality of groups of data lines.

16. (new) The data path circuit of claim 11, wherein each of the register files is only coupled to the single group of data lines in the plurality of data lines through a single port.

17. (new) The data path circuit of claim 11, wherein each of the register files is not coupled to at least one of the plurality of data lines.

18. (new) The data path circuit of claim 6, wherein each of the register files is only coupled to a single group of data lines in the plurality of data lines through a single port.

19. (new) The data path circuit of claim 6, wherein each of the register files is not coupled to at least one of the plurality of data lines.

20. (new) The data path circuit of claim 6, further comprising a plurality of registers coupled to the plurality of data path lines, the plurality of registers configured to store values from the plurality of data path lines so that the values are selectively available on the plurality of groups of data lines.